DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 24-27 and 46 are rejected under 35 U. S. C. 102(b) as being anticipated by Coomer (US 2003/0132527; hereinafter Coomer).

Regarding claims 24 and 46, Coomer discloses a semiconductor component comprising: a stack of semiconductor chips 300 (fig. 3), the semiconductor chips 310 being arranged in a manner fixed cohesively one on top of another, the semiconductor chips 310 comprising contact areas 320 (horizontal portion 320) extending as far as the edges of the semiconductor chips 310; and conductor portions 320 (vertical portion 320) extending from at least one upper edge to a lower edge of the edge sides of the semiconductor chips 310 and electrically connecting the contact areas 320 of the semiconductor chips of the semiconductor chip stack 300.

Regarding claim 25, Coomer discloses the semiconductor chips having two or more different chip sizes (fig. 3).

Regarding claim 26, Coomer discloses the semiconductor chips having a different number of contact areas at their edges (fig. 4A).

Regarding claim 27, Coomer discloses wherein the contact areas are arranged on one or more of the semiconductor edge sides, the semiconductor top side, and the semiconductor rear side so as to enable a freely selectable stacking order for the semiconductor chips forming the stack (fig. 3).

2. Claim 24-32 and 40-46 are rejected under 35 U. S. C. 102(b) as being anticipated by Pedersen (US 5,837,566; hereinafter Pedersen).

Regarding claims 24-32 and 40-46, Pedersen discloses a semiconductor component comprising: a stack of semiconductor chips (figs. 8B, 10A&10B), the semiconductor chips being arranged in a manner fixed cohesively one on top of another, the semiconductor chips 36 comprising contact areas 42 extending as far as the edges of the semiconductor chips 36 (fig. 8B); conductor portions 130 extending from at least one upper edge to a lower edge of the edge sides of the semiconductor chips 36 and electrically connecting the contact areas of the semiconductor chips of the semiconductor chip stack (fig. 10B); where the electrically conductive conductor portions 130 are arranged adhesively on the semiconductor chip edges, the semiconductor edge sides, the semiconductor top side and/or the semiconductor rear side with a freely selectable stacking order (fig. 10A&10B and col. 9, line 55 through col. 10, line 25); and where the conductor portions 130 comprise an adherent plastic resist which is filled with metallic nanoparticles and is electrically conductive (130 is a conductive epoxy filled with silver particle, see col. 9, lines 61-65).

Allowable Subject Matter

3. Claims 33-39 are allowed.

4. The following is an examiner's statement of reasons for allowance: the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including encapsulating the semiconductor stack with a layer made of a plastic resist which is filled with nanoparticles; and patterning the layer to form interconnect sections between the contact areas of the semiconductor chips stacked one on top of another.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

5. Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke H can

be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/DAVID VU/
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